Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): A clock signal generating circuit for receiving a phase-modulated input signal to generate a non-phase-modulated target clock signal, the clock signal generating circuit comprising:

a comparing circuit for generating a combining signal according to peak values of the input signal and comparing the combining signal with a reference voltage to generate a first protection signal; and

a phase lock loop (PLL) electrically connected to the comparing circuit for receiving the input signal and the first protection signal to generate the target clock signal that is a feedback to an input end of the phase lock loop, for driving the target clock signal synchronous to the input signal according to a first logic level of the ~~input~~ first protection signal, and for not driving the target clock signal synchronous to the input signal according to a second logic level of the ~~input~~ first protection signal to keep outputting the target clock signal.

2 (currently amended): The clock signal generating circuit of claim 1 wherein the comparing circuit comprises:

a hold circuit for receiving the input signal to obtain a peak signal and a bottom signal of the input signal;

a combining circuit electrically connected to the hold circuit for generating the combining signal according to voltage ~~difference~~ differences between the peak signal and the bottom signal; and

a comparator electrically connected to the combining circuit for comparing the combining signal with the reference voltage and outputting the first protection

signal according to a comparing result.

3 (original): The clock signal generating circuit of claim 2 wherein the hold circuit comprises:

a peak hold circuit for generating the peak signal according to the reference signal; and

a bottom hold circuit for generating the bottom signal according to the reference signal.

4 (original): The clock signal generating circuit of claim 1 further comprising:

a first band-pass filter for controlling the input signal to correspond to a predetermined frequency range before the input signal is inputted into the PLL and the comparing circuit; and

a first slicer having an output end electrically connected to the PLL for slicing the input signal into a square waveform.

5 (original): The clock signal generating circuit of claim 4 further comprising:

an automatic gain controller electrically connected to the first band-pass filter for adjusting the amplitude of the input signal by utilizing different gain values; and

a second band-pass filter having an input end electrically connected to the automatic gain controller and having an output end electrically connected to the first slicer, the second band-pass filter being used for controlling the amplified input signal to correspond to the predetermined frequency range.

6 (original): The clock signal generating circuit of claim 1 wherein if the voltage difference between the combining signal and the predetermined reference voltage is not larger than a threshold value, the first protection signal corresponds to the first

logic level.

7 (currently amended): The clock signal generating circuit of claim 1 wherein the first protection signal corresponds to the first logic level when the voltage difference between the combining signal and the predetermined reference voltage is not larger than a threshold value for ~~predetermined times~~ a predetermined period of time.

8 (original): The clock signal generating circuit of claim 1 wherein the first protection signal corresponds to the second logic level when the voltage difference between the combining signal and the predetermined reference voltage is larger than a threshold value.

9 (currently amended): The clock signal generating circuit of claim 1 wherein the first protection signal corresponds to the second logic level when the voltage difference between the combining signal and the predetermined reference voltage is larger than a threshold value for ~~predetermined times~~ a predetermined period of time.

10 (original): The clock signal generating circuit of claim 1 wherein the optical disc drive comprises an address in pre-groove decoder for predicting a timing that the input signal forms the phase modulation, and for generating a second protection signal before a predetermined time interval to the timing to control the target clock signal not to be synchronous with the input signal to maintain the target clock signal.

11 (currently amended): A clock signal generating method for generating a non-phase-modulated target clock signal according to a phase-modulated input signal, the clock signal generating method comprising:

determining whether ~~adjusting~~ to adjust the phase of the input signal to be synchronous with the phase of the target clock signal according to a first

protection signal, for outputting a control signal;

outputting a control voltage according to the control signal;

adjusting the frequency of the target clock signal according to the control voltage; and

generating the first protection signal according to voltage differences between a combining signal generated from peak values of the input signal and a reference voltage.

12 (original): The clock signal generating method of claim 11 wherein the step of generating the first protection signal comprises:

getting a bottom signal and a peak signal of the input signal;

generating the combining signal according to voltage differences between the peak signal and the bottom signal; and

comparing voltage differences between the combining signal and the predetermined reference voltage to output the first protection signal.

13 (original): The clock signal generating method of claim 11 wherein the input signal is compared with the target clock signal to drive the target clock signal synchronous with the input signal when the first protection signal corresponds to a first logic level, and the target clock signal is maintained without being driven to be synchronous with the input signal when the first protection signal corresponds to a second logic level.

14 (original): The clock signal generating method of claim 13 wherein if the voltage difference between the combining signal and the predetermined reference voltage is not larger than a threshold value, the first protection signal corresponds to the first logic level.

15 (currently amended): The clock signal generating method of claim 13 wherein the first

protection signal corresponds to the first logic level when the voltage difference between the combining signal and the predetermined reference voltage is not larger than a threshold value for ~~predetermined times~~ a predetermined period of time.

16 (original): The clock signal generating method of claim 13 wherein the first protection signal corresponds to the second logic level when the voltage difference between the combining signal and the predetermined reference voltage is larger than a threshold value.

17 (currently amended): The clock signal generating method of claim 13 wherein the first protection signal corresponds to the second logic level when the voltage difference between the combining signal and the predetermined reference voltage is larger than a threshold value for ~~several times~~ a predetermined period of time.

18 (original): The clock signal generating method of claim 17 further comprising:
predicting the timing when the input signal forms the phase modulation, and generating a second protection signal before a predetermined time interval to the timing to control the target clock signal not to adjust the input signal for maintaining the target clock signal.